

APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: PROTECTION CIRCUIT

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CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EV321180938US

July 24, 2003

Date of Deposit

PROTECTION CIRCUIT

TECHNICAL FIELD

[0001] This invention relates to computer systems and, more particularly, to methods and apparatus for providing high voltages in circuitry manufactured by processes typically used to provide low voltage tolerant integrated circuitry.

BACKGROUND

[0002] Flash EEPROM memory arrays have been used in personal computers as a type of long term memory. For example, a flash EEPROM memory array may be used in place of a hard disk drive as described in U.S. patent no. 5,822,781, entitled "Sector Based Storage Device Emulator Having Variable-Sized Sector", issued to S. Wells on Oct. 13, 1998, and assigned to the assignee of the present invention. Such a flash memory array provides a smaller, lighter, functional equivalent of a hard disk drive and is not as sensitive to physical damage. Such a flash memory array would be especially useful in portable computers, where space and weight are important considerations. However, these flash EEPROM memory arrays may also require much higher voltages and substantially more power than that directly available from the batteries of low power portable computers.

[0003] Typically, a flash memory array is subdivided into blocks and the erase mode may erase one or more blocks of memory cells. The flash memory cell may be erased by removing excess charge from the floating gate. The conventional method of erasing all the cells in a block of flash memory requires the application of 12 volts to the source terminals of all of the memory cells in the block while the drain terminals are left floating and the gate terminals are grounded. Flash memory cells may be programmed by placing excess charge on the floating gate to increase the threshold voltage of the flash memory cell. Programming is typically achieved by applying approximately 11-12 volts to the gate, 6-7 volts to the drain, and grounding the source terminal so that electrons are placed on the floating gate by hot electron injection. Flash memory cells can be read by applying a fixed voltage to the gate of the flash memory cell in order to determine whether the flash memory cell is in an erased or a programmed state. This technique senses the drain-to-source current, I_{ds} , for the flash memory cell. Reading a flash memory cell typically requires the application of 5 volts to the gate, 1 volt to the drain, and grounding the source terminal. Thus, typical voltages required for flash memory applications include 5 volts for the read mode and 6 and 12 volts for both the program and erase modes.

[0004] Power for the flash memory device can be provided by a Vcc line and a Vpp line. The Vcc line is the primary power source for the flash device. The supplemental voltage provided by supply line, Vpp, is typically needed only when writing or erasing the memory because of the higher voltages needed during those operations. Vcc can be approximately 5 volts. Vpp, however, might be 3.3, 5, or 12 volts.

[0005] When Vpp is large, a correspondingly large voltage stress is encountered by the field effect transistor devices that pass Vpp to the internal nodes of the Flash chip. The high voltage stresses in turn cause premature breakdown of the transistors. Accordingly, transistors capable of tolerating high voltage stresses are suitable for such applications. Field effect transistor devices with thick oxide layers are relatively tolerant to sustained voltage gradients across their gate oxide on the order of 12 volts. However, since such thick oxide devices have a low transconductance (low GM), they have to be made very large to minimize the voltage drop across them. Such transistors can occupy an undue amount of chip surface area and disadvantageously increase chip size and production cost.

[0006] Thin oxide transistor devices such as S devices and P devices occupy much less space on the chip, but generally are not capable of withstanding the voltage stress caused by direct coupling to a sustained power pad voltage. Over time, the large

voltage gradient can cause the oxide layers of such S and P devices to fail. For this reason, thick oxide transistor devices have typically been used in protection circuit applications.

DESCRIPTION OF DRAWINGS

[0007] FIG. 1 is a block diagram illustrating a computer system that can utilize the present invention;

[0008] FIG. 2 is a circuit and block diagram illustrating one embodiment of a protection circuit;

[0009] FIG. 3 is a logic diagram illustrating one embodiment of the switching logic identified in FIG. 2; and

[0010] FIG. 4 is a logic diagram illustrating one embodiment of the pull-down logic identified in FIG. 2.

[0011] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0012] The invention relates to circuits for protecting low voltage tolerant devices from sustained high voltages with thin-oxide transistor devices. Depicted in FIGS. 1 through 4 is an exemplary system for protecting the internal nodes of a flash EEPROM device from high power pad voltages, such as 12 volt power pad voltages. The protection circuit component interposes parallel connected thin oxide transistor devices between the power pad and the internal nodes of the flash EEPROM device.

The internal node voltage can be set at an acceptably low non-zero voltage by the threshold voltage drop across the transistor device or devices in one of the two branches. The other branch can be used to pass the full power pad voltage to the internal nodes when the EEPROM is in algorithm. That can be accomplished through the use of switching logic that selectively activates the transistor device in the second branch. Because the internal node voltage is set at a value substantially above zero, the transistor device in the second branch is not subjected to sustained voltage gradients on the order of 12 volts, which in turn permits the use of smaller thin oxide devices.

[0013] FIG. 1 shows a computer system 100 into which the present invention can be incorporated. The system 100 includes a central processor 110 which carries out the various instructions provided to the computer 100 for its operations. The central processor 110 is joined to a bus 120 adapted to carry information to various components of the system 100. Joined to the bus 120 is main memory 102 which is typically constructed of dynamic random access memory arranged in a manner well known to those skilled in the prior art to store information during a period in which power is provided to the system 100. Also joined to the bus 120 is read only memory 112 which may include various memory devices well known to those skilled in the art each of

which is adapted to retain a particular memory condition in the absence of power to the system 100. The read-only memory 112 typically stores various basic functions used by the processor 110 such as basic input/output processes and startup processes typically referred to as BIOS processes. Such read-only memory 112 may be constructed of flash EEPROM memory cells adapted to be modified as various ones of the BIOS processes used by a particular computer are changed. If the read-only memory 112 is constructed of flash EEPROM memory cells, it may be modified by running an update process on the computer itself to reprogram the values stored in the read-only memory 112. Typically, such flash EEPROM memory will include circuitry for programming and erasing the memory array.

[0014] Also connected to the bus 120 are various peripheral components such as long term memory 104 and circuitry such as a frame buffer 106 to which data may be written which is to be transferred to an output device such as a monitor 114 for display. The construction and operation of long term memory 104 (typically electro-mechanical hard disk drives) is well known to those skilled in the art. However, rather than the typical electro-mechanical hard disk drive, a flash EEPROM memory array may be used as the long term memory 104. Such flash EEPROM memory arrays are programmed and erased through techniques which utilize voltages greater than those typically available to the

integrated circuits of more advanced portable computers. Such flash EEPROM memory arrays typically include circuitry for programming and erasing the memory array. Consequently, in accordance with the present invention, such long term memory arrays as well as memory 112 may provide circuitry for generating high voltages from the lower voltages available from the batteries typically utilized with such computers. In order to generate accurate high voltages for programming and erasing such flash EEPROM memory arrays the present invention introduces voltage regulation circuitry needed to generate precise programming voltages.

[0015] Circuitry is also shown in FIG. 1 by which power may be supplied through a power bus 130 to various components of the system 100. This includes in the exemplary embodiment a power control circuit 108 which controls the various states for applying power to the system 100 and a battery 116 which may be utilized in a portable computer for furnishing power to the system 100 under control of the power control circuitry 108. In any particular arrangement, the power control circuitry 108 may actually be a part of a particular portion of the circuit of FIG. 1. For example, if the read only memory were to be constructed of flash EEPROM memory devices, power control circuitry 108 including voltage reference circuitry in

accordance with the present invention might be a physical portion of the read only memory block.

[0016] FIG. 2 illustrates a circuit diagram for one embodiment of a protection circuit 200 particularly suited for use in connection with the flash EEPROM devices discussed above. Power supply pad 201 supplies Vpp to the protection circuit 200. Vpp can be supplied by charge pump circuits such as those described in U.S. Patent No. 5,553,030, entitled "Method and Apparatus for Controlling the Output Voltage Provided by a Charge Pump," issued to Kerry D. Tedrow et al. on September 3, 1996, and assigned to the assignee of the present invention, or other known means. Vpp can be 12 volts or another voltage sufficient to effectuate programming and erase operations in a flash EEPROM connected to node 202. Power supply pad 201 maintains node 204 at Vpp.

[0017] Transistor devices 206 and 208 are special N-type devices referred to as S devices. S devices are basically N-type devices having a very low threshold voltage level. The use and manufacture of S devices are described in detail in U.S. Patent No. 5,057,715, entitled "CMOS Output Circuit Using A Low Threshold Device," issued to Larsen et al. on October 15, 1991, and assigned to the assignee of the present invention. Device 206 is connected in diode fashion to node 204. The gate and drain of device 206 are connected to node 204. The source of

device 206 is connected to a second diode-configured transistor device 208. The gate and drain of device 208 are connected to the source of device 206. The source of transistor device 208 is connected to node 202. In the depicted embodiment, both S devices have a threshold voltage of about 0.8 volts with transistor body effect.

[0018] P device 210 is a p-channel transistor device, which has an oxide layer significantly thinner than the M and O devices described above. The source of device 210 is connected through node 204 to the power supply pad 201 and the source of n-channel device 206. The drain of transistor device 210 is connected to node 202 and the source of device 208. The gate of device 210 is connected to switching logic 300, which is described in more detail hereinbelow.

[0019] Also connected to node 202 is a constant current source 214 and a N-type transistor device 216. In a preferred embodiment, current source 214 maintains the branch current at 2-5 microamperes. The drain of transistor device 216 is connected to node 202. The gate of device 216 is connected to pull-down logic 400, which is also described in more detail hereinbelow.

[0020] In operation, the circuit of FIG. 2 protects devices connected to node 202 from V_{pp} and passes V_{pp} when the associated flash EEPROM device is in an erase or program

algorithm. A small sub-threshold current 218 flows through the diode-connected S devices 206 and 208. The threshold voltage drops across devices 206 and 208 set the voltage of node 202 at $V_{pp}-2V_{ts}$, where V_{ts} refers to the threshold voltage of the S devices. Constant current source 214 bleeds the sub-threshold current off node 202, thereby maintaining the node voltage at approximately $V_{pp}-2V_{ts}$. Accordingly, the drain-gate voltages of P device 210 is only $2V_{ts}$, which is well below the maximum tolerable steady state voltage stress.

[0021] Switching logic 300 maintains the gate voltage at V_{pp} when the chip is not in algorithm. During program or erase modes, logic 300 grounds the gate of P device 210, which permits V_{pp} to pass to the internal nodes of the flash chip. After the algorithm is complete, logic 300 brings the gate of device 210 back to V_{pp} , which turns device 210 off and prevents V_{pp} from passing to node 202. Pull down logic 400 then pulses the gate of device 216 with a 20-30 nanosecond V_{cc} pulse to activate device 216. When device 216 is active, approximately $2V_{ts}$ is dropped between the device's drain and source. The voltage of node 202 is thus dropped immediately back to $V_{pp}-2V_{ts}$. At the terminating edge of the pull down logic pulse, device 216 goes inactive and the circuit 200 resumes steady state, or non-algorithm, operation.

[0022] FIG. 3 is a logic diagram depicting a circuit that can be used as switching logic 300. Inputs 302, 304 are control or test bits. Input 306 from a micro-controller (not shown) is coupled to an inverter 308. Input 306 is 0 when the EEPROM is in algorithm. Inputs 302, 304 and inverter 308 are coupled to NOR gate 310. Accordingly, whenever one of the test bits is 1 or the EEPROM is in algorithm, the output from the NOR gate is 0. The NOR gate output is one input for level shifter 312. The other is a low voltage trigger 318 which is 1 when an unacceptably low Vcc is observed, and 0 otherwise. The remaining input 320 to level shifter 312 is tied to the power pad 201. Whenever the input from the NOR gate or low voltage trigger is 1, the output 314 of the level shifter 312 is Vpp and the bar output 316 is 0. When both are low, output 314 is 0 and the bar output is Vpp. The bar output 316 is conductively coupled to the gate of device 210. Accordingly, switching logic 300 takes the gate of transistor device 210 low when the EEPROM is in a program or erase mode, thereby passing Vpp to the internal nodes of the EEPROM device.

[0023] Turning now to FIG. 4, depicted is an exemplary embodiment of pull-down logic 400. Delay chain 402 accepts as input the inverted output of NOR gate 310. Delay chain 402 is preferably configured so as to provide about a 100 nanosecond delay. The output of the delay chain 402 is thus 0 under steady

state conditions and 1 when the EEPROM is in algorithm. That output is tied to AND gate 406 and inverter 408, which is in turn tied to delay chain 410. The output of delay chain 410, which is 1 under steady state conditions and 0 when the computer is in algorithm, is also coupled to AND gate 406. Accordingly, when the EEPROM enters algorithm, the first input of the AND gate goes high after the delay period set by delay chain 402. After a delay set by chain 410, preferably about 50 to 100 nanoseconds, the second input to the AND gate is taken low. The net effect is that a digital Vcc pulse is output to the gate of n-device 216, which in turn pulls down the voltage of node 202 after completion of the algorithm.

[0024] Referring again to FIG. 2, the constant current source 214 may be provided by coupling known current generators to the gates of one or more n-type transistor devices whose drains are connected to node 202. Suitable logic can be used to provide Vcc to the gates of transistor devices in the current generator, thereby transmitting current, preferably on the order of 10 microamperes, to the gates of the transistor devices connected to node 202.

[0025] In other embodiments, the protection circuit of the instant invention may be used in different systems to protect low-voltage tolerant devices from high voltage sources. For instance, the circuit 200 can be used to protect circuits on

parts of the chip other than the pad. The protection circuit 200 may also be readily modified to work with variable voltage sources or power supply pads. S devices 206 and 208 may be substituted with other transistor devices having acceptable threshold voltages, and can be advantageously replaced with other thin oxide layer devices. The leaker current source 214 may be substituted with variable controlled voltage sources, transistor devices having sub-threshold current, or an RC circuit that maintains node 202 at a reduced voltage during steady state operation. P device 210 can be advantageously replaced with other thin oxide devices which pass an acceptably high percentage of the source or power pad voltage. P device 210 can be replaced with thick oxide M and O devices or a combination of transistor devices. Logic 300 can be substituted with any suitable switching circuit that activates or disables transistor devices in protection circuit 200 to permit the passage of a substantial fraction of the supply voltage. For example, level shifter 312 can be replaced with a resistor divider circuit coupled to N devices, wherein the resistor and N devices are configured such that the output of switching logic 300 is identical but no transistor device experiences stress from a V_{pp} input. The pull-down circuit 216, 400 can be advantageously replaced with any suitable array of transistor devices that serve to maintain the node voltage 202 at a desired

level after completion of an algorithm. Those skilled in the art will appreciate that leaker 214 and pull-down device 216 can in certain circumstances be combined into one transistor device having an appropriate sub-threshold current. The leaker and/or pull-down elements may be eliminated entirely if the other devices are selected so that the appropriate node voltage is maintained at the drain of device 210.

[0026] Aspects of the invention provide for one or more of the following advantages. The use of high GM, thin oxide devices greatly reduces the size of the transistor devices, and accordingly reduces the overall cost and size of the chip. The protection circuit can provide for the maintenance of a relatively constant flash chip node voltage when not in algorithm. The circuit can also provide rapid transition from V_{pp} to steady state node voltage after an algorithm is complete. The circuit also optionally permits the passage of V_{pp} through a single transistor device with the use of a single switch. Moreover, the protection circuit is much less complex and involves fewer components than previous protection devices, which further reduces material and production costs.

[0027] As used herein, the term "thin oxide transistor" refers to a device having an oxide layer substantially thinner than 320 Angstroms. Thick oxide devices typically have a gate oxide that is 320 to 340 Angstroms thick. The thin oxide P

devices used in the depicted embodiments preferably have a gate oxide thickness of less than about 250 Angstroms, and most preferably in range of 170 to 190 Angstroms.

[0028] The terms "coupled" or "joined," are used with reference to components that are directly or indirectly joined together. If one or more intermediary components are inserted between two referenced components, the referenced components are still "coupled" or "joined," as those terms are used herein.

[0029] The term "parallel connection," as used herein, refers to a topology in which current flow is divided among two or more channels from a common starting point or header. Accordingly, circuit elements are considered to be in parallel even if the outputs of the elements are not directly coupled together.

[0030] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.